Claims 1-3, 5, 14-18, 23, and 24 have been amended to overcome rejection under 35 U.S.C. 112. The Examiner is thanked for his very helpful suggestions in this matter.

All Claims are believed to be in condition for Allowance and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1, 2, 4, and 10-14 as being anticipated by Hung et al is requested in view of Amended Claim 1 and in accordance with the following remarks.

A key feature of Applicants' invention is that it is very important not to use etch stop layers with low dielectric constant layers (see top of page 2 of the Specification). It is important that the dielectric constant of the dielectric layer through which the damascene opening is etched be less than 2.5. If an etch stop layer is used within the dielectric layer, the effective dielectric constant of the dielectric layer will increase above 2.5. In Hung et al, a nitride etch stop layer 16 is used within the dielectric layer 14/16/20 (see col. 9, lines 7-10 and Figs. 5-10). Claim 1 has been amended to claim the important dielectric constant of less than 2.5 from dependent Claim 4. It is believed that this important difference in dielectric

layer composition differentiates Applicants' detailed now claimed invention from Hung et al.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1, 2, 4, and 10-14 as being anticipated by Hung et al is requested in view of Amended Claim 1 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 3, 5, 7, 8, 15-18, 21-27, and 30 as being unpatentable over Hung et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the following remarks.

As discussed above, a key feature of Applicants' invention is that it is very important not to use etch stop layers with low dielectric constant layers. It is important that the dielectric constant of the dielectric layer through which the damascene opening is etched be less than 2.5. In Hung et al, a nitride etch stop layer 16 is used within the dielectric layer 14/16/20 (see col. 9, lines 7-10 and Figs. 5-10). Claim 1 has been amended to claim the important dielectric constant of less than 2.5 from dependent Claim 4. Claim 15 has been amended to claim no etch stop layer (taught at the top of page 2 of the Specification). Claim 24 has been amended to claim the specific etching gases from

Claim 28. There is no teaching or suggestion in Hung et al that an etch stop layer not be used, now claimed in Claims 1 and 15. There is also no teaching or suggestion in Hung et al of the specific etching gases taught in Applicants' first etching step and now claimed in Claim 24.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 3, 5, 7, 8, 15-18, 21-27, and 30 as being unpatentable over Hung et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 19, and 28 as being unpatentable over Hung et al and further in view of Tang et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the following remarks.

It is agreed that Hung et al does not teach the specific etching gases taught in Applicants' first etching step. As discussed above, Hung et al also does not teach or suggest not using an etch stop layer (as now claimed in Claim 15) so that the dielectric constant remains lower than 2.5 (as now claimed in Claim 1). Claim 24 has been amended to claim the specific etching gases from Claim 28. It is agreed that Tang et al teach using CF_4, O_2, and Ar in etching. However, they

also teach adding C_2F_6 (col. 9, line 52 - col. 10, line 3). This teaches away from Applicants' invention because Applicants have found that high polymer gases such as C_2F_6 cause spiking (see bottom of page 8 of the Specification). It is an object of Applicants' invention to prevent spiking. Tang's etching recipe would cause spiking because of the presence of C_2F_6.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 19, and 28 as being unpatentable over Hung et al and further in view of Tang et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9, 20, and 29 as being unpatentable over Hung et al and further in view of Chan et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the following remarks.

It is agreed that Hung et al does not teach the specific etching gases taught in Applicants' second etching step. As discussed above, Hung et al also does not teach or suggest not using an etch stop layer (as now claimed in Claim 15) so that the dielectric constant remains lower than 2.5 (as now

claimed in Claim 1). It is agreed that Chan et al teach using CF_4 in etching. However, it is not agreed that Chan et al use O_2 and Ar in etching this stop layer. Etching chemistry is taught for each layer. There is no teaching that a subsequent gas is added to previous gases. For example, see col. 6 lines 16-19 and lines 22-25. In the first instance, CHF_3 and O_2 are used to etch a mask layer 54. In the second instance, O_2 and Ar etch the dielectric layer 50. Since these are consecutive steps and O_2 is mentioned in both instances, it is reasonable to assume that O_2 is meant to be used where it is mentioned and not meant to be used where it is not mentioned. Chan et al teach etching the bottom stop layer using CF_4 (col. 6, lines 50-52). No mention is made here of O_2 and Ar, so it is reasonable to assume that O_2 and Ar are not to be used in this particular etching step.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9, 20, and 29 as being unpatentable over Hung et al and further in view of Chan et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the remarks above.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while

the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Specification and Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Chen not find that the Claims are now Allowable that the Examiner call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

Rosemary L. S. Pike. Reg # 39,332

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the first paragraph on page 3 with the following:

U.S. Patent 6,123,862 to Donohoe et al discloses an etching process for high aspect ratio openings. U.S. Patent 6,156,64[2]3 to Chen et al teaches a dual damascene process. U.S. Patents 6,159,661 to Huang et al, 6,096,655 to Lee et al, and 6,127,089 to Subramanian et al show dual damascene processes using low dielectric constant materials.

IN THE CLAIMS

Please amend the Claims as follows:

1. (AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a contact region [to be contacted] in or on a substrate;

depositing a liner layer overlying said contact

region [to be contacted];

depositing a dielectric layer overlying said liner layer wherein no portion of said dielectric layer has a dielectric constant higher than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said contact region [to be contacted] wherein said first etching comprises a high F/C ratio etch chemistry, high power, and low pressure; and

second etching said liner layer within said damascene opening to expose said contact region [to be contacted] wherein said second etching comprises a high F/C ratio etch chemistry, low power, and low pressure to complete formation of said damascene opening in said fabrication of said integrated circuit device.

2. (AMENDED) The method according to Claim 1 wherein said contact region [to be contacted] is [selected from the group containing:] a gate electrode, a source region, a drain region[s], [and] or a metal line.

3. (AMENDED) The method according to Claim 1 wherein said liner layer is [selected from the group containing] silicon nitride [and] or silicon carbide and has a thickness of between about 300 and 700 Angstroms.

Please cancel Claim 4.

5. (AMENDED) The method according to Claim 1 wherein said dielectric layer is [selected from the group containing:] Black Diamond [and] or organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

14. (AMENDED) The method according to Claim 13 wherein said metal layer is [selected from the group containing] copper [and] or aluminum-copper alloys.

15. (AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a contact region [to be contacted] in or on a substrate;

depositing a liner layer overlying said contact region [to be contacted];

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5 and wherein no etch stop layer is used within said dielectric layer;

first etching said damascene opening through said

dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr; and

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr to complete formation of said damascene opening in said fabrication of said integrated circuit device.

16. (AMENDED) The method according to Claim 15 wherein said contact region [to be contacted] is [selected from the group containing:] a gate electrode, a source region, a drain regions, [and] or a metal line.

17. (AMENDED) The method according to Claim 15 wherein said liner layer is [selected from the group containing] silicon nitride [and] or silicon carbide and has a thickness of between about 300 and 700 Angstroms.

18. (AMENDED) The method according to Claim 15 wherein said dielectric layer is [selected from the group

containing:] Black Diamond [and] or organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

23. (AMENDED) The method according to Claim 22 wherein said metal layer is [selected from the group containing] copper [and] or aluminum-copper alloys.

24. (AMENDED) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing a contact region [to be contacted] in or on a substrate;

depositing a liner layer overlying said contact region [to be contacted];

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry of CF_4, O_2, and Ar gases, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr;

second etching said liner layer within said damascene opening to expose said region to be contacted

wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr;

depositing a barrier metal layer within said damascene opening;

depositing a copper layer overlying said barrier metal layer; and

polishing down said copper layer and said barrier metal layer to leave said barrier metal layer and said copper layer only within said damascene opening to complete said copper metallization in said fabrication of said integrated circuit device.

25. (AMENDED) The method according to Claim 24 wherein said contact region [to be contacted] is [selected from the group containing:] a gate electrode, a source region, a drain regions, [and] or a metal line.

26. (AMENDED) The method according to Claim 24 wherein said liner layer is [selected from the group containing] silicon nitride [and] or silicon carbide and has a thickness of between about 300 and 700 Angstroms.

27. (AMENDED) The method according to Claim 24 wherein said dielectric layer is [selected from the group containing:] Black Diamond [and] or organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.